

INTEGRATED CIRCUIT MEMORY DEVICES

Abstract of the Disclosure

An integrated circuit memory device and a method of manufacturing the same are provided. A plurality of word line structures are formed on predetermined portions of a semiconductor substrate on which an active region is defined. Word line contact plugs are formed between the word line structures on the active region.

5 An insulating layer is deposited on the semiconductor substrate on which the word line contact plugs are formed. Bit line structures are formed on the insulating layer so as to be in electrical contact with some of the word line contact plugs. An interlayer insulating layer is deposited on the bit line structures. An etch stopper is formed on the interlayer insulating layer. Storage node contact holes are formed by

10 etching predetermined portions of the interlayer insulating layer and the etch stopper to expose word line contact plugs not yet exposed. Storage node contact plugs are formed so as to fill the storage node contact holes. Storage node electrodes are formed to be in electrical contact with the storage node contact plugs. The remaining etch stopper and the interlayer insulating layer between the storage node

15 contact plugs are selectively removed. A dielectric layer is formed on the exposed surfaces of the storage node contact plugs and the storage node electrodes. A plate electrode is formed on the dielectric layer and extending between the storage node contact plugs.